

SEMICONDUCTOR DEVICE WITH INDUCTIVE COMPONENT
AND METHOD OF MAKING

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1 SEMICONDUCTOR DEVICE WITH INDUCTIVE COMPONENT
2 AND METHOD OF MAKING
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4

5 Background of the Invention
6

7 The present invention relates in general to semiconductor
8 devices and, more particularly, to integrated circuits formed
9 with inductive components such as planar inductors and
10 transformers.
11

12 Many semiconductor devices integrate both active and
13 passive components on the same die in order to reduce the
14 manufacturing cost of electronic systems. For example, many
15 wireless communication systems are fabricated with an
16 integrated circuit that includes a low noise radio frequency
17 input amplifier and a bandpass or impedance matching filter
18 formed on the same semiconductor die. The filter often
19 includes a planar inductor or transformer which is integrated
20 on the semiconductor die along with the amplifier's active
21 transistors.
22

23 However, most integrated electromagnetic devices such as
24 inductors suffer from a low quality factor owing to a low
25 resistivity semiconductor substrate used to avoid a latchup

1 condition of the integrated circuit. The proximity of the
2 inductor to the low resistivity substrate induces parasitic
3 image currents in the substrate that load the inductor and
4 reduce its quality factor. Moreover, the semiconductor
5 material used to form the substrate typically has a high
6 dielectric constant which produces a high parasitic
7 capacitance of the inductor, which reduces its frequency
8 response and degrades the performance of the integrated
9 circuit.

10
11 Hence, there is a need for an integrated circuit and
12 method of fabrication that provides a high quality factor
13 inductive component in order to maintain a low system cost and
14 a high performance of the integrated circuit.

Brief Description of the Drawings

FIG. 1 shows a top view of an integrated circuit; and

FIG. 2 shows a top view of a portion of a dielectric region of the integrated circuit;

FIG. 3 shows a cross-sectional view of a selected portion of the integrated circuit after a first processing step;

FIG. 4 shows a cross-sectional view of the selected portion of the integrated circuit after a second processing step;

FIG. 5 shows a cross-sectional view of the selected portion of the integrated circuit after a third processing step;

FIG. 6 shows a cross-sectional view of the selected portion of the integrated circuit after a fourth processing step;

FIG. 7 shows a cross-sectional view of the selected portion of the integrated circuit after a fifth processing step;

1 FIG. 8 shows a cross-sectional view of the selected
2 portion of the integrated circuit after a sixth processing
3 step;

4
5 FIG. 9 shows a cross-sectional view of the selected
6 portion of the integrated circuit after a seventh processing
7 step;

8
9 FIG. 10 shows a cross-sectional view of the selected
10 portion of the integrated circuit after an eighth processing
11 step;

12
13 FIG. 11 is a schematic diagram of a portion of the
14 integrated circuit including a transistor and a transformer;

15
16 FIG. 12 is a top view of a first portion of the
17 transformer formed in the dielectric region of the integrated
18 circuit;

19
20 FIG. 13 is a top view of a second portion of the
21 transformer; and

22
23 FIG. 14 is a top view of the transformer showing the
24 relationship of the first and second portions of the
25 transformer.

Detailed Description of the Drawings

In the figures, elements having the same reference numbers have similar functionality.

FIG. 1 is a top plan view of an integrated circuit 10, showing a semiconductor substrate 11 having a top surface 32 for defining an active region 12 and a low permittivity dielectric region 14. Active region 12 is formed with active circuitry that includes transistors and/or other active components. Components of integrated circuit 10 are configured to operate at a frequency of at least six gigahertz. In one embodiment, substrate 11 is formed with silicon.

Dielectric region 14 is formed within a boundary 15 of an insulating material having a reduced permittivity structure. Hence, dielectric region 14 is ideal for forming passive components such as inductors which have a low parasitic capacitance and a high degree of electrical isolation from substrate 11, and therefore a high quality factor and frequency response. A recessed region (76) is defined by edges 70 and 71 of a surface 73 formed on a bottom surface of substrate 11 as described below to further enhance the quality factor of passive components formed on dielectric region 14.

1 A recessed region 93 is used to align integrated circuit
2 10 on a die attach flag with other similarly configured
3 semiconductor dice to provide a circuit with multiple
4 interconnected semiconductor dice. Recessed region 93 has a
5 sloped edge defined by corners or edges 91 and 92 as described
6 in further detail below.

7

8 FIG. 2 is a top view of integrated circuit 10 showing a
9 portion of dielectric region 14 in further detail. A
10 dielectric material 17 is formed on substrate 11 so as to
11 define an array of holes or cavities 16. Cavities 16
12 typically are filled with a gaseous material or vacuum which
13 has a low dielectric constant, thereby reducing the effective
14 permittivity and enhancing the frequency response of
15 components formed on dielectric region 14. Dielectric
16 material 17 is preferably formed to a depth of at least five
17 micrometers in order to electrically isolate passive
18 components from being loaded by substrate 11. In one
19 embodiment, dielectric material 17 comprises thermally grown
20 silicon dioxide formed to a depth of about thirty micrometers
21 and formed in accordance with a method disclosed in pending
22 U.S. patent application serial number 09/527,281, filed on
23 March 17, 2000 by the same inventor, Robert B. Davies, and
24 entitled "Die Attachment and Method". The effective width of
25 cavities 16 is about 1.2 micrometers and cavities 16 are

1 separated by dielectric material 17 having a typical width of
2 0.4 micrometers.

3

4 Passive components such as inductors and transformers
5 often occupy a large die area. To accommodate these passive
6 components, the die area occupied by dielectric region 14 is
7 similarly large. For example, in one embodiment, dielectric
8 region 14 occupies a die area of about one hundred thousand
9 square micrometers. Therefore, dielectric region 14 is formed
10 with dielectric material 17 comprising thermally grown silicon
11 dioxide, which has a high mechanical strength in order to
12 resist cracking during the manufacturing process and while
13 operating integrated circuit 10 over its specified temperature
14 range.

15

16 FIG. 3 is a cross-sectional view of a selected portion of
17 integrated circuit 10, showing details of active region 12 and
18 dielectric region 14 after a first processing step. A region
19 29 is formed adjacent to a bottom surface 34 of substrate 11
20 with a low resistivity p-type semiconductor material, which
21 provides a low minority carrier lifetime that avoids a latchup
22 condition of integrated circuit 10. In one embodiment, region
23 29 has a resistivity of about 0.01 ohm-centimeters. An
24 epitaxial region 19 is formed to overlie region 29 and extend
25 to top surface 32. Epitaxial region 19 comprises a higher

1 resistivity p-type semiconductor material suitable for forming
2 active circuitry. In one embodiment, epitaxial region 19 has
3 a resistivity of about ten ohm-centimeters.

4

5 Active region 12 includes a transistor 20 operating as an
6 n-channel metal oxide semiconductor field effect transistor.
7 Heavily doped n-type regions 21 and 22 are formed at top
8 surface 32 within epitaxial region 19 to function as a source
9 21 and drain 22 of transistor 20, respectively. A conductive
10 material such as doped polysilicon is formed on top surface 32
11 to function as a source electrode 23 and a drain electrode 24
12 for providing electrical contact to source 21 and drain 22,
13 respectively. A layer of conductive material is disposed over
14 a gate dielectric 26 as shown to function as a control or gate
15 electrode 25 of transistor 20. In one embodiment, transistor
16 20 is a component of a high frequency amplifier operating at
17 about six gigahertz.

18

19 Dielectric region 14 is formed by selectively etching
20 semiconductor material from substrate 11 to form an array of
21 columnar openings and then thermally oxidizing the remaining
22 semiconductor material to form dielectric material 17 to
23 define sidewalls of cavities 16. In one embodiment,
24 dielectric material 17 extends within substrate 11 from
25 surface 32 to a surface 36 to a depth $D=30.0$ micrometers. A

1 cap layer 38 is formed by depositing a semiconductor oxide
2 material to seal off cavities 16. Devices in active region
3 12, such as transistor 20, typically are fabricated after
4 dielectric material 17 is thermally formed in order to avoid
5 subjecting these active devices to high temperatures that
6 could adversely modify their performance.

7

8 Cavities 16 typically contains a gaseous material such as
9 air that has a dielectric constant approaching one. In one
10 embodiment, dielectric material 17 comprises thermally grown
11 silicon dioxide, which has a dielectric constant of about 3.8.
12 When combined with the effective relative permittivity of
13 about 1.0 that characterizes cavities 16, the overall
14 effective relative permittivity or dielectric constant of
15 dielectric region 14 is about 2.5.

16

17 An interlevel dielectric layer 28 is formed over top
18 surface 32 to overlie active region 12 and dielectric region
19 14. In one embodiment, dielectric layer 28 comprises silicon
20 dioxide deposited to a thickness of about five thousand
21 angstroms between top surface 32 and an interconnect surface
22 31 of dielectric layer 28. Dielectric layer 28 may be
23 subjected to a chemical mechanical polishing or similar
24 process to provide a high degree of planarity of surface 31.

25 FIG. 4 is a cross-sectional view of the selected portion of

1 integrated circuit 10 after a second processing step. A
2 photoresist layer 42 is formed over surface 31 and patterned
3 as shown. Integrated circuit 10 is then subjected to a
4 standard anisotropic etch to remove material from dielectric
5 layer 28 and cap layer 38 sufficient to open up those cavities
6 16 which are not covered by photoresist layer 42. An
7 isotropic etching step is then used to selectively remove
8 sidewall material from the opened cavities 16 to form a trench
9 40. In one embodiment, dielectric region 14 comprises silicon
10 dioxide, and an etchant with a high selectivity for silicon
11 dioxide over silicon is used. Hence, region 29 functions as
12 an etch stop to ensure that a bottom surface 39 of trench 40
13 is adjacent to region 29. In one embodiment, trench 40 is
14 formed to a width W of about thirty micrometers.

15
16 To ensure that dielectric material 17 is completely
17 removed from bottom surface 39 so that region 29 is exposed,
18 the isotropic etching step is timed to slightly overetch
19 dielectric material 17. As a result, one or two rows of
20 cavities 16 that underlie photoresist layer 42 may be removed
21 and sidewalls 41 may not be perfectly vertical in shape.
22 Since the width of dielectric material between cavities 16 is
23 about 0.4 micrometers while the width of trench 40 is much
24 greater, e.g., thirty micrometers, a small degree of
25 overetching is not considered deleterious and can increase the

1 effective surface area of trench 40 over what would be
2 achieved if sidewalls 41 were perfectly vertical. The
3 increased surface area has an advantage of reducing the
4 effective resistance of an embedded conductor, particularly
5 when the resistance is determined by the skin effect such as
6 when operating at a high frequency greater than about one
7 gigahertz.

8

9 To obtain the benefits of low relative permittivity,
10 dielectric region 14 is formed to extend beyond the area
11 occupied by trench 40 so that one or more cavities 16 lies
12 adjacent to trench 40. In one embodiment, cavities 16 are
13 considered to lie adjacent to trench 40 where the effective
14 dielectric constant of dielectric region 14 is at least ten
15 percent lower than the dielectric constant of dielectric
16 material 17.

17

18 FIG. 5 is a cross-sectional view of the selected portion
19 of integrated circuit 10 after a third processing step.
20 Photoresist layer 42 is removed and a conductive layer 44 is
21 deposited to a thickness of about five hundred angstroms to
22 cover surface 31 as well as sidewalls 41 and bottom surface 39
23 of trench 40. In one embodiment, layer 44 is formed with a
24 metal such as platinum, titanium or cobalt which can combine
25 with silicon to form a silicide.

FIG. 6 is a cross-sectional view of the selected portion of integrated circuit 10 after a fourth processing step. Integrated circuit 10 is subjected to an etching step that removes layer 44 from regions adjacent to surface 31 and sidewalls 41. Along bottom surface 39 of trench 40, the conductive material used to form layer 44 combines with semiconductor material from region 29 to form a silicide layer 51 that is resistant to the etching step. In one embodiment, platinum is used to form layer 44, region 29 is formed with silicon, and the etching step is performed using an aqua regia or similar etchant. The aqua regia etchant removes elemental platinum from regions adjacent to surface 31 and sidewalls 41, but the platinum adjacent to bottom surface 39 combines with silicon from region 29 to form conductive platinum silicide which functions as silicide layer 51 which is not removed by the aqua regia etch.

17

FIG. 7 is a cross-sectional view of the selected portion of integrated circuit 10 after a fifth processing step. A thin dielectric material is deposited over integrated circuit 10 and then anisotropically etched to form spacers 43 along sidewalls 41 of trench 40. In one embodiment, spacers 43 are formed with silicon nitride to a thickness of about two thousand angstroms.

1 To ensure an adequate barrier for subsequent etching
2 processes, a plating voltage V_{P1} is applied to bottom surface
3 34 to produce a plating current I_{P1} that flows through region
4 29 and silicide layer 51 to electroplate additional platinum
5 over silicide layer 51, thereby forming a layer 46 that
6 increases the overall thickness of conductive material over
7 bottom surface 39. In one embodiment, platinum is plated to
8 form layer 46 to a thickness of about five thousand angstroms.
9 Plating voltage V_{P1} typically is applied uniformly over bottom
10 surface 34 to ensure a uniform distribution of plating current
11 within trench 40 and within trenches of other integrated
12 circuit dice (not shown) fabricated on the same wafer as
13 integrated circuit 10.

14
15 Plating voltage V_{P1} is then applied to electroplate a high
16 conductivity material such as copper upwardly from layer 46 to
17 fill trench 40 to a depth of about 0.5 micrometers below the
18 plane of surface 31 to form a conductor 47. Where the high
19 conductivity material is chemically reactive, a conductive
20 barrier layer 48 is formed over conductor 47 with a less
21 chemically active, low resistance material such as platinum to
22 enclose conductor 47 to avoid contaminating other portions of
23 integrated circuit 10 during subsequent processing steps.
24 Conductor 47 and barrier layer 48 are effectively connected in
25 parallel to function as an inductor 50. In one embodiment,

1 barrier layer 48 comprises platinum plated to a surface 49
2 which is substantially coplanar with surface 31. Such
3 coplanarity avoids metal thinning when covering a large step
4 and therefore facilitates making electrical connection to
5 relatively thick inductor 50 using standard, relatively thin
6 integrated circuit metallization.

7

8 The described plating method is not limited to forming
9 inductors, but typically is used to concurrently form other
10 integrated circuit passive components and structures which
11 have a low parasitic capacitance and high frequency response.
12 For example, the plating method is used to form low series
13 resistance capacitor plates, bonding pads and the like.

14

15 Note that the above described plating scheme provides a
16 conductive path through region 29 that couples plating voltage
17 V_{P1} from bottom surface 34 of substrate 11 to bottom surface 39
18 to plate the high conductivity material that forms conductor
19 47. Hence, plating voltage V_{P1} is applied to a first surface,
20 e.g., bottom surface 34, to plate high conductivity material
21 from a second surface, e.g., bottom surface 39, to form
22 conductor 47 at or adjacent to a third surface of substrate
23 11, e.g., surface 31. Most if not all existing plating
24 schemes apply a plating voltage at the edge of the top surface
25 of a semiconductor wafer in order to plate a passive component

1 on the top surface. Such schemes typically require that a
2 blanket seed layer be formed on the top surface to receive the
3 plating voltage and an additional photoresist layer be formed
4 and patterned to define the plated region. However, to insure
5 uniform plating, voltage drops must be minimized across the
6 seed layer, which limits the magnitude of the plating current
7 and increases the time needed for completing the plating step,
8 thereby increasing the fabrication cost.

9

10 With the plating scheme shown in FIG. 7, virtually equal
11 resistances are maintained between bottom surface 34 and the
12 various trenches to be plated, which allows a higher magnitude
13 of plating current to flow without producing voltage drops
14 that can reduce plating uniformity. The higher plating
15 current results in a shorter plating time, which reduces the
16 fabrication cost of integrated circuit 10. Moreover, a seed
17 layer is not needed for plating inductor 50, which further
18 reduces the fabrication cost.

19

20 FIG. 8 is a cross-sectional view of the selected portion
21 of integrated circuit 10 after a sixth processing step.
22 Dielectric layer 28 is selectively etched through and filled
23 with a conductive material such as copper, tungsten, or
24 aluminum to form a via 55 that electrically contacts drain
25 electrode 24 of transistor 20. In one embodiment, vias 55 are

1 formed with tungsten to a thickness of about 0.5 micrometers.
2 Alternatively, dielectric layer 28 is selectively etched to
3 form a contact opening that exposes drain electrode 24 for
4 contacting directly to an interconnect trace.

5

6 A conductive film is deposited over dielectric layer 28
7 and selectively etched to form a standard integrated circuit
8 interconnect metallization trace 57 as shown to electrically
9 couple drain electrode 24 through via 55 to inductor 50. In
10 one embodiment, trace 57 is formed with copper plated to a
11 thickness of about 0.5 micrometers. As described above,
12 surface 49 of inductor 50 is formed to be substantially
13 coplanar with surface 31, so there is little or no step
14 between dielectric layer 28 and inductor 50. As a result of
15 the coplanarity, trace 57 is formed to directly contact
16 inductor 50 at surface 49 while maintaining a substantially
17 constant thickness. That is, there is little or no thinning
18 of trace 57 due to poor step coverage because there is little
19 or no height difference or step between surface 31 and surface
20 49. Since there is little or no thinning, trace 57 has a low
21 resistance and a high reliability of integrated circuit 10 is
22 achieved.

23

24 Depending on the application and/or the complexity of
25 integrated circuit 10, additional interconnect layers may be

1 formed over trace 57 by alternately depositing and selectively
2 etching interlevel dielectric and conductive films in
3 accordance with standard integrated processing.

4

5 A dielectric layer 58 is formed over trace 57 and/or the
6 additional interconnect layers. Dielectric layer 58 is
7 patterned and etched to form openings which are filled with a
8 conductive material to produce an array of vias 59 that
9 contact trace 57. In one embodiment, dielectric layer 58
10 comprises polyimide formed to a thickness of about ten
11 micrometers and vias 59 comprise plated copper.

12

13 Geometrically, inductor 50 is formed as a spiral inductor
14 whose windings lie in a lower level plane 33 running parallel
15 to surface 31. To maintain a small die size while forming a
16 high performance transformer or an inductor with a higher
17 inductance, one or more additional windings are formed in an
18 upper level plane 37 running parallel to surface 31 as
19 follows.

20

21 A conductive material is deposited over dielectric layer
22 58 to form a seed layer 54 that functions as a plating
23 electrode. A thick photoresist layer 56 is formed over seed
24 layer 54 and then exposed and developed to form a trench 62
25 over vias 59. A plating voltage V_{P2} is applied to bottom

1 surface 34 and coupled through region 29, inductor 50, trace
2 57 and vias 59 to seed layer 54 to plate a conductive material
3 such as copper within trench 62 to form an inductor 250. The
4 thickness of inductor 250 preferably is at least five
5 micrometers to provide a low series resistance. In one
6 embodiment, inductor 250 is formed to a thickness of about
7 thirty micrometers. Depending on the interconnection scheme,
8 magnetic fields produced by a varying current flowing through
9 inductors 50 and 250 are electromagnetically coupled so that
10 inductors 50 and 250 combine to produce an increased
11 inductance or may be coupled to interact to function as a
12 transformer.

13
14 The steps used for forming inductor 250 can also be used
15 to form traces for interconnecting multiple dice mounted in a
16 plane in the same package. In that case, plating voltage V_{P2}
17 is applied to seed layer 54 to plate the conductive material
18 to form inductor 250 and the interconnect traces.

19
20 FIG. 9 shows a cross-sectional view of the selected
21 portion of integrated circuit 10 after a seventh processing
22 step. Photoresist layer 56 is removed and seed layer 54 is
23 etched to remove the portion not covered by inductor 250. A
24 passivation layer 61 is formed over dielectric layer 58,
25 inductor 250 and other exposed portions of integrated circuit

1 10. The effective parasitic capacitance of inductor 250 is a
2 function of the thickness and permittivity of passivation
3 layer 61. Hence, in applications where it is advantageous to
4 form inductors 50 and 250 with generally equal parasitic
5 capacitances, the thickness of passivation layer 61 can be
6 adjusted to set the effective interwinding permittivity of
7 inductor 250 to match or equal the effective interwinding
8 permittivity of inductor 50. For example, in an embodiment
9 where windings of inductor 250 are spaced thirty micrometers
10 apart, passivation layer 61 comprises polyimide with a
11 relative permittivity of about 2.8 and a thickness of about
12 twenty-six micrometers to produce a relative interwinding
13 permittivity of about 2.5 to match the effective permittivity
14 of dielectric region 14.

15
16 FIG. 10 shows a cross-sectional view of the selected
17 portion of integrated circuit 10 after an eighth processing
18 step. Bottom surface 34 is patterned and substrate 11 is
19 selectively etched to form recessed region 93 defined by edges
20 91 and 92 as indicated above. In one embodiment, substrate 11
21 is etched so that edges 91 and 92 bound a side surface 94
22 extending to a surface 35 whose height is about four hundred
23 micrometers above the height of bottom surface 34. Substrate
24 11 preferably is etched isotropically to produce etched side
25 surface 94 along a crystallographic plane of substrate 11 at a

1 predictable angle A of about 54.7 degrees with respect to the
2 plane of bottom surface 34.

3

4 Surface 35 is patterned and etched to remove material
5 from region 29 to form recessed region 76 to extend from
6 surface 35 to silicide layer 51 and/or surface 36 of
7 dielectric material 17. In one embodiment, silicide layer 51
8 comprises platinum silicide and material is removed from
9 region 29 with an etchant that includes potassium hydroxide.
10 Even if platinum silicide is removed from silicide layer 51 by
11 the potassium hydroxide etchant, virtually zero platinum is
12 consumed from layer 46, which therefore provides a complete
13 etch stop. Silicon dioxide resists etching with potassium
14 hydroxide and therefore functions as a natural etch stop to
15 allow a degree of overetching that ensures that recessed
16 region 76 extends to silicide layer 51 and surface 36, i.e.,
17 that silicide layer 51 and surface 36 are exposed. The
18 etching step typically is preferential, which produces an
19 etched surface 73 along a crystallographic plane of substrate
20 11 at angle B of about 54.7 degrees with respect to the plane
21 of surface 35.

22

23 Because the conductive material of region 29 is removed
24 to form recessed region 76, substantially zero parasitic image
25 currents are induced in substrate 11 by changing magnetic

1 fields induced by currents flowing through inductors 50 and
2 250. As a result, inductors 50 and 250 have higher quality
3 factors than previous integrated inductors. Moreover, there
4 is effectively zero parasitic capacitance to substrate 11,
5 which increases the frequency response of inductors 50 and
6 250.

7

8 Integrated circuit 10 is mounted to a die attach pad 72
9 of an integrated circuit package which includes a pedestal 74
10 having side surface 75 formed at angle A for mounting
11 substrate 11. In one embodiment, pedestal 74 does not extend
12 above surface 35, so that recessed region 76 forms a cavity
13 between an upper surface 77 of pedestal 74, which reduces
14 loading of inductors 50 250. In another embodiment, material
15 is removed from pedestal 74 in a region adjacent to surface 77
16 to further increase the volume of the cavity formed by
17 pedestal 74 and recessed region 76. Recessed region 76
18 preferably has a height of at least thirty micrometers. In
19 one embodiment, the height of recessed region 76, i.e., the
20 distance between surface 35 and bottom surface 39 is about one
21 hundred micrometers. Recessed region 76 preferably has a
22 height of at least thirty micrometers. In one embodiment, the
23 height of recessed region 76, i.e., the distance between
24 surface 35 and bottom surface 39 is about one hundred
25 micrometers.

1 Note that a gap is formed between surfaces 75 and 94 and
2 between surfaces 78 and 35 as shown to reduce thermal and/or
3 mechanical stress between substrate 11 and die attach pad 72.
4 The gap may be fully or partially filled with excess die
5 attach material such as gold, solder, or electrically
6 conductive epoxy used to bond surface 35 to surface 77. The
7 die attach material preferably has a high thermal
8 conductivity.

9

10 FIG. 11 is a schematic diagram of the selected portion of
11 integrated circuit 10 including transistor 20 and a
12 transformer 90 formed in dielectric region 14.

13

14 Transformer 90 has a primary winding 150 that includes a
15 lower portion formed in lower level plane 33 which is
16 designated as inductor 50 and an upper portion formed in upper
17 level plane 37 and designated as inductor 250. Inductor 50
18 has an electrode 82 for coupling through trace 57 to drain
19 electrode 24 of transistor 20, and an electrode 83 for
20 serially coupling to inductor 250. An electrode 81 is used to
21 contact other circuitry (not shown). A secondary winding 160
22 has a lower portion formed in lower level plane 33 which is
23 designated as inductor 60, and an upper portion formed in
24 upper level plane 37 which is designated as an inductor 260.
25 Inductor 60 has an electrode 84 for external coupling and an

1 electrode 85 for serially coupling to inductor 260. Inductor
2 260 is further coupled to a center tap electrode 86 of
3 transformer 90. A secondary winding 180 has a lower portion
4 formed in lower level plane 33 and designated as an inductor
5 80, and an upper portion formed in upper level plane 37 and
6 designated as an inductor 280. Inductor 80 is coupled to
7 center tap electrode 86 and serially coupled to inductor 280
8 at an electrode 87. Inductor 280 further includes an
9 electrode 88 for external coupling.

10
11 FIG. 12 is a top view of a first portion of transformer
12 90 as formed in dielectric region 14 showing features formed
13 in lower level plane 33, including planar spiral inductors 50,
14 60 and 80. Even though inductors 50, 60 and 80 are formed
15 concurrently in lower level plane 33, they are shown with
16 different fill codes to more clearly show their geometric
17 symmetry.

18
19 Primary winding 150 conducts a primary current I_p through
20 inductor 50 from electrode 82 to electrode 83. Current I_p
21 induces a secondary current I_{s1} in secondary winding 160 and a
22 secondary current I_{s2} in secondary winding 180. Secondary
23 current I_{s1} flows through inductor 60 from electrode 85 to
24 electrode 84, while secondary current I_{s2} flows through
25 inductor 80 from electrode 87 to electrode 86 as shown.

1 Electrodes 82-87 include vias similar to vias 55 and/or vias
2 59 as appropriate for internally and/or externally coupling to
3 transformer 90. For example, electrode 82 comprises one or
4 more of vias 55 for coupling to trace 57 and transistor 20 as
5 shown, while electrode 83 includes one or more of vias 59 for
6 coupling inductor 50 to inductor 250. In one embodiment, the
7 width of inductors 50, 60 and 80 is thirty micrometers and the
8 separation between adjacent inductors is thirty micrometers.

9 Inductor 60 is formed as an outer winding while inductor 80 is
10 formed as an inner winding. Inductor 50 is formed to lie
11 between inductors 60 and 80 so that primary winding 150 is
12 close coupled to both secondary windings 160 and 180. In one
13 embodiment, inductors 60 and 80 are adjusted to have
14 substantially equal lengths to produce substantially equal
15 inductances.

16
17 FIG. 13 is a top view of a second portion of transformer
18 90 as formed over dielectric region 14 showing features formed
19 in upper level plane 37. Individual inductors that are formed
20 in upper level plane 37 are shown with different fill codes to
21 more clearly show the current flow through transformer 90.
22 The second portion of transformer 90 is configured similarly
23 to the first portion with three planar spiral windings as
24 shown which are electrically coupled to windings formed in
25 lower level plane 33. Primary current I_p flows from inductor

1 50 through electrode 83 and inductor 250 and to other
2 circuitry (not shown) at electrode 81. Secondary current I_{s1}
3 flows from inductor 260 at electrode 85 through inductor 60 to
4 center tap electrode 86. Secondary current I_{s2} flows from
5 center tap electrode 86 through inductor 80 to electrode 87
6 and through inductor 280 to electrode 88 for external
7 coupling.

8

9 Inductor 260 is formed as an inner winding while inductor
10 280 is formed as an outer winding and inductor 250 is formed
11 to lie between inductors 260 and 280. Hence, inductor 60 of
12 secondary winding 160 is formed as an outer winding while
13 inductor 260 is formed as an inner winding. Similarly,
14 inductor 80 of secondary winding 180 is formed as an inner
15 winding while inductor 280 is formed as an outer winding. In
16 one embodiment, inductors 60 and 80 are adjusted to have
17 substantially equal lengths to produce substantially equal
18 inductances. Alternatively, transformer 90 can be configured
19 so that a difference in the inductances of inductors 260 and
20 80 is compensated by a comparable difference in the
21 inductances of inductors 60 and 280, so that secondary
22 windings 160 and 180 have substantially equal or matched
23 inductances.

24

25 Hence, transformer 90 is formed so the geometries of the

1 upper and lower portions of transformer 90 are selected to
2 provide total inductances of secondary windings 160 and 180
3 which are substantially equal. A greater length of inductor
4 60 over inductor 80 in the lower portion of transformer 90 is
5 offset by a greater length of inductor 280 over inductor 260
6 in the upper portion of transformer 90. Conversely, a greater
7 length of inductor 260 may be offset by a similarly greater
8 length of inductor 280. The parasitic capacitances of
9 inductors 60 and 80 are balanced with the respective parasitic
10 capacitances of inductors 260 and 280 by adjusting the
11 thickness of passivation layer 61. As a result, transformer
12 90 is suitable for use as a high performance balun in a
13 wireless communication device to convert a single ended six
14 gigahertz radio frequency signal through primary winding 150
15 to a balanced differential signal across secondary windings
16 160 and 180.

17

18 FIG. 14 is a top view of transformer 90 showing the upper
19 and lower portions of windings 150, 160 and 180 in one view to
20 more clearly indicate the relationship between windings formed
21 on lower level plane 33 and upper level plane 37. Note that
22 although inductors 50, 60, 80, 250, 260 and 280 are formed as
23 described above, each is shown with a unique fill code to more
24 clearly indicate the symmetry of windings 150, 160 and 180.

